Low power design: additional complexity due to:

Low power design elements:

1. Clock gating, data-gating – power shutoff PSO
2. Multiple VDD domains and creation of power islands
3. Isolation cells + Level shifters
4. Retention logic
5. Secondary PG routing – due to Always ON cells in collapsible domains
6. Insert Power switches/ Head or Foot (GDHS) or Block head switch (BHS).
7. UPF / CPF to capture power intent and its validation before use.
8. Inrush current analysis + PDN complexity + Voltage Droop analysis
9. Early Bump planning for multiple VDD, ESD signoff and protection and package routing
10. Conformal Low Power CLP signoff for all domain crossings

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